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 Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
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 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
 Volume 19, Issue 7, July 2000 Page(s):808 - 814
 Digital Object Identifier 10.1109/43.851996
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(212 KB\)](#) IEEE JNL
- ☐ 3. **Energy and peak-current per-cycle estimation at RTL**
 Gupta, S.; Najm, F.N.;
 Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
 Volume 11, Issue 4, Aug. 2003 Page(s):525 - 537
 Digital Object Identifier 10.1109/TVLSI.2002.800534
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(721 KB\)](#) IEEE JNL
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 Gupta, S.; Najm, F.N.;
 Low Power Electronics and Design, 1999. Proceedings. 1999 International Syr
 1999 Page(s):103 - 105
[AbstractPlus](#) | Full Text: [PDF\(228 KB\)](#) IEEE CNF
- ☐ 5. **Energy-per-cycle estimation at RTL**
 Gupta, S.; Najm, F.N.;
 Low Power Electronics and Design, 1999. Proceedings. 1999 International Syr
 1999 Page(s):121 - 126
[AbstractPlus](#) | Full Text: [PDF\(448 KB\)](#) IEEE CNF
- ☐ 6. **Analytical model for high level power modeling of combinational and seq**
 Gupta, S.; Najm, F.N.;
 Low-Power Design, 1999. Proceedings. IEEE Alessandro Volta Memorial Worl
 4-5 March 1999 Page(s):164 - 172

Digital Object Identifier 10.1109/LPD.1999.750417

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7. Power Macromodeling For High Level Power Estimation

Gupta, S.; Najm, F.N.;

Design Automation Conference, 1997. Proceedings of the 34th

June 9-13, 1997 Page(s):365 - 370

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